IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: J. Orion Pritchard et al.	Atty Dkt No.: ALTRP116/A1364
Application No.: 10/775,966	Examiner: Siek, Vuthe
Filed: February 9, 2004	Group: 2825
Title: METHODS AND APPARATUS FOR VARIABLE LATENCY SUPPORT	Confirmation No: 2158

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PREAPPEAL REQUEST FOR REVIEW

Applicant requests review of the final rejection mailed June 28, 2007 in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated below.

REMARKS

Claims 1-27 are pending. The Examiner rejected claims 1-27 including independent claims 1, 11, and 21 under 35 U.S.C. 120(e) as being anticipated by Oh (6,996,016 B2). The Examiner also rejected claims 1-7, 11-17, and 21-27 separately under 35 U.S.C. 102(e) as being anticipated by Wingard (6,725,313). Neither Oh nor Wingard are believed to teach or suggest all of the elements of the claims. To facilitate prosecution, the independent claims were amended in a preliminary amendment filed with an RCE to recite "providing a selection mechanism to a user to have the primary component access the secondary component using fixed latency or variable latency and receiving a selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency." Despite the significant amendments to the claims and corresponding substantive arguments, the Examiner issued a First Office Action Final. The finality of the First Office Action is believed improper. Furthermore, neither Oh nor Wingard teach or suggest "providing a selection mechanism to a user" or "receiving a selection from a user to have the primary component issue a plurality of reads to the

secondary component using variable latency." The Examiner does not respond to the claim amendments directly, but is believed to argue that they are simply inherent.

Oh notes "the system bus 106 comprises a bi-directional line 114 (shown in phantom) that transmits a WAIT_DQS signal and a plurality unidirectional transmission lines propagating conventional control and command signals. Such conventional control and command signals comprise, among other such signals, a Clock (CLK) signal, an Address (e.g., 21-bit address word A20-A0) signal, an Address Valid (ADV) signal, a Write Enable (WE) signal, and a Chip Select (CS) signal (all discussed below in reference to FIGS. 3-7)." (column 4, lines 12-24) Oh also states that a double data rate (DDR) burst PSRAM memory device can operate in a "variable latency mode in Read cycle and a fixed latency mode in Write cycle or in the variable latency mode in both Read and Write cycles." (Summary) When a particular mode is being used, a particular line is asserted. "In the fixed latency mode, the first data input D0 is always needed at the same time after a burst command regardless of internal state of the memory 104. Specifically, FIG. 4 depicts the CLK, A20 A0, ADV#, WE#, CS#, WAIT_DQS, and DQ15 DQ0 signals (graphs 1 7, respectively) versus time." (Figure 4 Description) Specific burst lengths are described for a system that is configured to use the memory in either mode. "In the fixed latency mode, the first data input D0 is always needed at the same time after a burst command regardless of internal state of the memory 104. Specifically, FIG. 4 depicts the CLK, A20 A0, ADV#, WE#, CS#, WAIT_DQS, and DQ15 DQ0 signals (graphs 1 7, respectively) versus time." (Figure 3 Description).

The Applicants acknowledge that there are components that can operate in either fixed or variable latency mode. As noted in the present application, "In one example, the data memory 17 can support variable latency or fixed latency." (page 7, lines 23-24) However, the techniques of the present invention recognize that supporting both variable latency and fixed latency using a system bus can be highly inefficient in many particular circumstances. Oh appears to support this notion as Oh goes into great length to describe burst lengths, timing relationships, signal assertions, in a complex bus fabric that allows the DDR SDRAM to operate in either fixed latency or variable latency modes for read or write operations. The configured system can sometimes use the DDR SDRAM in fixed latency mode for writes and at other times use the DDR SDRAM in variable latency mode for writes.

By contrast, the techniques of the present invention recognize that manually configuring a system to support these multiple modes of operation can be highly inefficient, as it creates bus modules that consume a large amount of resources. The resources may be trivial in an application specific integrated circuit (ASIC) system as described in Oh. However, the resources

are significant in a programmable chip as recited in the claims. Consequently, the techniques of the present invention allow a user to select a either a variable latency or a fixed latency configuration of a secondary component for a component that actually supports both. For example, the system provides "a selection mechanism to a user to have the primary component access the secondary component using fixed latency or variable latency" as recited in the claims. The user then selects either a fixed latency or a variable latency way of operation and the system bus is optimized to support that mode of operation. For example, the system receives "a selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency in response to providing the selection mechanism" as recited in various claims.

The Examiner argues that this providing a selection mechanism and receiving a selection from the user is inherent in Oh. The Applicants respectfully disagree. Oh does not provide any selection mechanism to a user to select either a fixed latency mode of operation or a variable latency mode of operation. In fact, Oh goes to great lenghts to describe a system that can support both. No user input selection is required, taught, or even suggested. Oh seems to teach that no selection mechanism needs to be provided because it has a system that can beneficially support both.

By contrast, the techniques of the present invention recognize that programmable chip resource usage can be made more efficient by configuring a system based on a user selection. "Figure 4 shows an architecture that supports fixed latency. Figure 5 shows an architecture that supports variable latency with the addition of a data valid line." (page 13, lines 23-24) "In some instances, a user can select, parameterize, and connect components automatically using the programmable chip tool. A user can select whether components should support fixed or variable latency and appropriate control lines are generated to support the desired configuration." (page 15, lines 25-29)

The Examiner also relies on Wingard to teach the elements of the claims. The Examiner argued that the Applicants did not address Wingard in the prior response. The Applicants did address Wingaard. Although Wingard shows a master and a slave along with connection lines, Wingard does not teach or suggest "generating interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module support a system having both fixed and variable latency components" or "receiving information ... and generating an interconnection module."

Wingard only describes "fixed latency" in one place. "In one embodiment, shared communications bus 1012 supports a bus protocol that is a framed, time division multiplexed, fully pipelined, fixed latency communication protocol using separate address, data and connection identification wires." (Figure 5 description) Wingard also only describes "variable latency" in a single place. "In one embodiment, shared communications bus 1012 supports a bus protocol that is a framed, time division multiplexed, fully pipelined, fixed latency communication protocol using separate address, data and connection identification wires." (Figure 5 description) It is not even clear that Wingard describes a secondary component that supports both fixed and variable latency. Without such a component, there can be not user selection of either fixed or variable latency operation. There can be no system receiving selection information to have a secondary component operate in variable latency mode based on the selection. Wingard can teach no generation of an interconnection module as recited in the claims. Again, generating an interconnection module or interconnection circuitry is not inherent. As noted above, primary and secondary components along with buses may be selected and placed without any "receiving information... and generating an interconnection module." Many conventional implementations including Wingard are believed to use this approach.

Claims 7, 17, and 27 also recite an interconnection mechanism comprising "simultaneous multiple primary component fabric." Neither Oh nor Wingard teach or suggest this recitation. Oh shows a detailed bus with control, clock, data, lines. Wingard shows a conventional bus. However, neither of these buses are a simultaneous multiple primary component fabric. These shared buses do not support access of two separate secondary component by two separate primary component simultaneously. The standard Oh and Wingard bus controls are believed to restrict access to a bus to one selected primary component at a time. As noted in the present application "Figure 3 is a diagrammatic representation showing one example of a system using secondary side arbitration, sometimes referred to as slave side arbitration, simultaneous multiple primary components, or simultaneous multiple masters. A system using individual arbitrators that correspond to individual secondary components accessible by more than one primary component is referred to herein as a secondary side arbitration system. The secondary side arbitration system no longer requires a bus or a system bus arbitrator that prevents a second primary component from accessing a second secondary component when a first primary component is accessing a first secondary component." (page 11, lines 6-14)

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. I am the attorney or agent acting under 37 CFR 1.34

Respectfully submitted,
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APPENDIX A: SELECTED PENDING CLAIMS

1. (Previously Presented) A method for configuring on a programmable chip, the method comprising:

receiving information associated with a primary component, the primary component having either fixed latency or variable latency characteristics;

receiving information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component;

providing a selection mechanism to a user to have the primary component access the secondary component using fixed latency or variable latency;

receiving a selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency, and

generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components.

7. (Previously Presented) The method of claim 1, wherein interconnection circuitry comprises a simultaneous multiple primary component fabric.

11. (Previously Presented) A system for configuring a programmable chip, the system comprising:

an input interface configured to receive information associated with a primary component and information associated with a secondary component, the secondary component configurable as either a fixed latency or a variable latency component, wherein the secondary component is operable to respond to requests from the primary component;

an output interface configured to provide a selection mechanism to a user to have the primary component access the secondary component using fixed latency or variable latency, wherein the input interface receives a selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency in response to providing the selection mechanism; and

a processor configured to generate interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines for the programmable chip, wherein the interconnection module supports a system having both fixed and variable latency components.